

# EL698R ACICD LABORATORY

## Lab 3

### CMOS OP Amp Design

#### Week 7, 8

(Prepared by: Wen-Yaw Chung, Electronic Eng. Dept, Chung-Yuan Christian University)

## I. Introduction

The purpose of this lab is to introduce the student to a generic CMOS OP Amp design via the HSPICE simulation and CADENCE layout tools. Your goal will be to design a two-stage CMOS OP Amp with the buffer stage for later analog signal processing application.

In the 1<sup>st</sup> part of this lab, you will have a suggested schematic of the proposed CMOS OP Amp and the advised design specifications. How to optimize your OP Amp design will be considered on the electrical parameters such as a high low-frequency gain, good phase margin, high slew rate, lower power dissipation, minimum device size and cell layout area.

Two kinds of biasing skills will be used in the output stage, one is the internal bias comes from the 1<sup>st</sup> stage's output, and the other is the external bias given by the bandgap reference studied in the **lab2**. You should compare the simulation results from two biasing techniques studied as above. Final conclusion should be given in the lab report.

## II. Schematics and Specifications of the proposed CMOS OP Amp

### A. Design Specifications of the proposed CMOS OP Amp

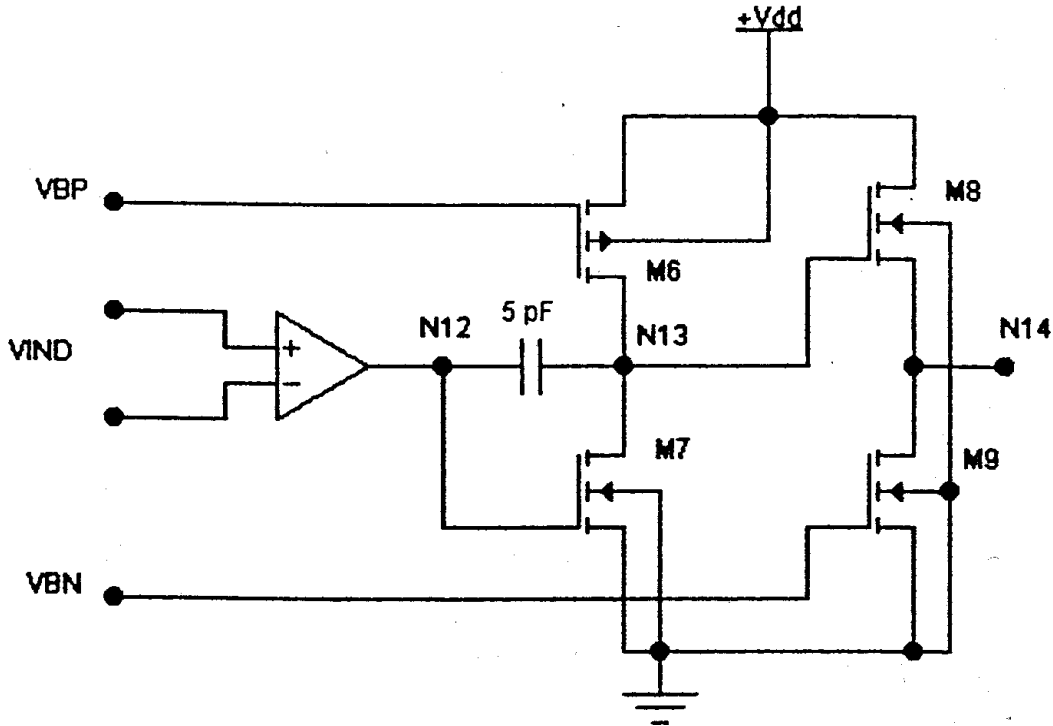
Nominal Operating Conditions: 5V, @25°C

Major design specifications:

- DC gain: 70dB, Phase margin:  $\geq 50^\circ$
- Slew rate:  $\geq 2V/\mu s$
- Bias current of the differential stage: 80 $\mu A$ , gain stage: 160 $\mu A$ , buffer stage: 320 $\mu A$
- Bias current of the self-bias circuit: 20 $\mu A$
- Loading condition: max. 10pF

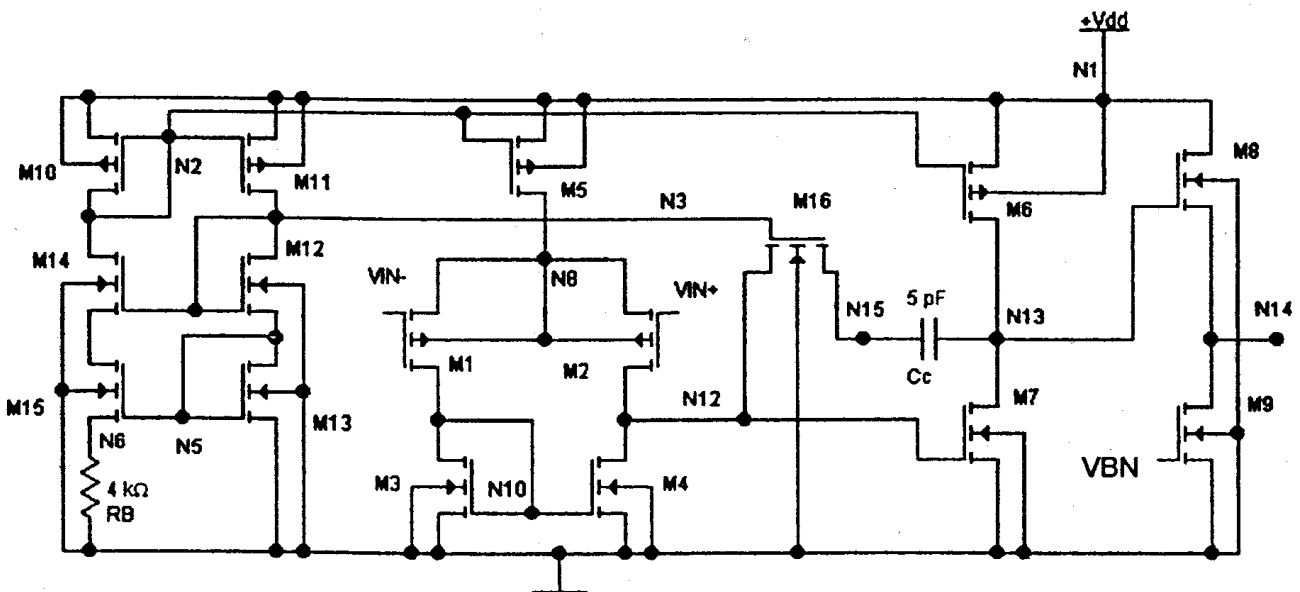
### 1. Top-view Schematic of the CMOS OP Amp shown in Fig.1

For internal usage, the op amp is typically used in a two-stage configuration, the two-stage op amp with the buffer stage is used for external usage.



Differential Input Stage      Second Gain Stage ( Inverting Amp)      Output Buffer  
Fig.1

### B. The Schematic of the Two-stage CMOS OP Amp with the Output Buffer



Self-bias Circuit      Differential stage      Compensation      Gain stage      Output buffer  
Fig. 2

**Self-bias circuit** – cascaded current mirrors consist of M10, M11, M12, M13, M14, M15, and RB, the bias current is set up by  $V_{RB}/R_B$

**Differential stage** – P-input driver pair M1, M2 and NMOS current mirror, M3, M4.

**Gain stage** – inverting amplifier consists of M6 and M7.

**Output buffer** – source follower consists of M8 and M9, the VBN is supplied by the output of the reference generator or the differential stage.

**Compensation components** –  $C_c$  for pole splitting and M16 for zero cancellation.

### III. Design Assignments

1. By using the hand calculation and analytic method, to find the proper sizes of all transistors for the two-stage op amp with the output buffer shown in Fig. 2. In order to find the optimized VBN value, connect the VBN node to the differential stage's output first.
2. Do the pre-layout simulation for the op amp and list the simulation results. Complete the layout of the op amp, the common-centroid and parallel MOSFET segment layout skills are suggested for better matching performance.
3. Post layout simulations of corner cases (TT, SS, FF, SF and FS) are necessary to study the worst case performance. (5V &  $0^\circ\text{C}$ -- $70^\circ\text{C}$  range)
4. Do the transient analysis for the op amp using two different biasing techniques (internal VBN & external VBN biases) for the slew rate and setting time parameters.
5. Hand in all design results including hand calculation, SPICE input netlist, operating point data and output graphical files.

#### **IV. Questions**

- A. Discuss the simulation results for the two different VBN bias techniques**
- B. Briefly describe other compensation skills can be used in CMOS OP Amp design.**
- C. List at least three applications of CMOS OP Amp.**

#### **V. References**

- [ A ] P. R. Gray & R. G. Meyer, Analysis and Design of Analog Integrated Circuits, 2<sup>nd</sup> edition, John Wiley & Sons, 1984.
- [ B ] D. A. Johns and K. Martin, Analog Integrated Circuit Design, John Wiley & Sons, Inc., Chap. 5, 1997.

\*low output impedance op with internal bias (4-5-99) \*

\*opa1.spi – 1998/5/21 12:03:22 PM

\*

.GLOBAL GND 1

\*2=VPB 11=PIN 9=NIN 14=OUT

x1 11 14 14 OPA1

\*VB VPB GND dc 3.669726

\*1=VDD

VDD 1 GND dc 5

VIN+ 11 GND dc 2.49949 AC 1

+PWL(0u 2 10us 2 10.01us 3 20u 3 20.01u 2 31u 2)

VIN- 9 GND dc 2.5

.....

.SUBCKT OPA1 11 9 14

M10	2	2	1	1	P	W=25	L=1.6	
M11	3	2	1	1	P	W=25	L=1.6	
M14	2	3	4	GND	N	W=25	L=1.6	
M12	3	3	5	GND	N	W=25	L=1.6	
M15	4	5	6	GND	N	W=25	L=1.6	M=4
M13	5	5	GND	GND	N	W=25	L=1.6	
RB	6	GND	4K					
M5	8	2	1	1	P	W=50	L=1.6	M=6
M1	10	9	8	1	P	W=50	L=1.6	M=6
M2	12	11	8	1	P	W=50	L=1.6	M=6
M3	10	10	GND	GND	N	W=50	L=1.6	M=3
M4	12	10	GND	GND	N	W=50	L=1.6	M=3
M6	13	2	1	1	P	W=50	L=1.6	M=10
M8	1	13	14	GND	N	W=50	L=1.6	M=6
M7	13	12	GND	GND	N	W=50	L=1.6	M=6
M9	14	12	GND	GND	N	W=50	L=1.6	M=10
Cc	15	13	5p					
M16	15	3	12	GND	N	W=50	L=1.6	M=2

.END OPA1

\*

\*.options nomod nopage scale=1e-6 nxx brief post=2 probe

.options nomod nopage numdgt=6 captab scale=1e-6 brief post=2

\*\*\*\*\*

\*.pz V(14) vin+

\*.ac dec 10 1 1000meg

\*.op

\*.noise v(14) vin+ 4

\*.print ac vm(14) vdb(14) vp(14)

\*.print noise onoise inoise

\*\*\*\*\*

\*.dc VIN+ 2.49940 2.49954 0.000004

\*.dc vin+ 2.48 2.54 0.005

\*.print dc v(14) l(x1.m3) l(x1.m4) l(x1.m7) l(x1.m9)

\*\*\*\*\*

.tran 0.2u 40u start=9u sweep cload 0 10p 10p

.print tran v(14) l(x1.m3) l(x1.m4) l(x1.m7) l(x1.m9)

Cl 14 GND cload

.param cload=10p

\*\*\*\*\*

.protect

.inc 'c:\meta\96\spice\model\umc\umc49.tt'

\*.inc 'c:\meta\96\spice\model\umc\bjt.mod'

.unprotect

.end